Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Original). Method for the production of individual monolithically integrated semiconductor circuits, which have a component structure on the front face of a substrate that has been reduced in thickness, and a metallized substrate back face, as well as electrical connections between the metallic substrate back face and conductive surfaces on the front face, by way of passage holes through the substrate, from a wafer containing a plurality of separate component structures, wherein

a) the wafer is attached to a rigid carrier after completion of the front face component structures, with the front face surface, by means of an attachment layer, over its entire area,

b) the substrate is reduced to the desired thickness,

c) the passage holes through the substrate are produced up to the conductive surfaces on the front face,

d) the separating trenches between the monolithic semiconductor circuits are produced up to or into the intermediate layer,

e) the back face metallization, including the electrical connections through the passage holes, is produced,

f) the semiconductor circuits are individually released

from the rigid carrier and individually processed further.

Claim 2 (Currently Amended). Method as recited in claim 1, ~~characterized in that~~ wherein an adhesive material is used for the attachment layer.

Claim 3 (Currently Amended). Method as recited in claim 2, ~~characterized in that~~ wherein an adhesive material having a lower adhesion to the front face surface of the wafer at a higher temperature is used.

Claim 4 (Currently Amended). Method as recited in claim 2 ~~or 3~~, ~~characterized in that~~ wherein the individual release of the semiconductor circuits from the carrier is performed mechanically, overcoming the adhesion force of the attachment material to the front face of the wafer.

Claim 5 (Currently Amended). Method as recited in ~~one of~~ claim~~s~~ 1 ~~to 4~~, ~~characterized in that~~ wherein the substrate is reduced in thickness to a thickness of less than 100 µm.

Claim 6 (Currently Amended). Method as recited in ~~one of~~ claim~~s~~ 1 ~~to 5~~, ~~characterized in that~~ wherein the separating trenches are produced by means of a photolithographic etching

process.

Claim 7 (Currently Amended). Method as recited in ~~one of~~ claim~~s~~ 1 ~~to 6~~, ~~characterized in that~~ wherein a protective layer is applied on the front face of the wafer.

Claim 8 (Currently Amended). Method as recited in claim 7, ~~characterized in that~~ wherein a lateral under-etching of the substrate is produced in the front face protective layer of the wafer.

Claim 9 (Currently Amended). Method as recited in ~~one of~~ claim~~s~~ 1 ~~to 8~~, ~~characterized in that~~ wherein the deposition of the back face metallization is performed after production of the separating trenches.

Claim 10 (Currently Amended). Method as recited in ~~one of~~ claim~~s~~ 6 ~~to 9~~, ~~characterized in that~~ wherein a common photolithographic mask is used for the production of the passage holes and the separating trenches.

Claim 11 (Currently Amended). Method as recited in ~~one of~~ claim~~s~~ 1 ~~to 10~~, ~~characterized in that~~ wherein an electrical function test of the semiconductor circuits is performed after separation.

Please add the Abstract of the Disclosure attached hereto.